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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,873	07/24/2003	Shigeo Kigo	P23801	9272

7055 7590 07/07/2005

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EXAMINER	
ABDULSELAM, ABBAS I	

ART UNIT.	PAPER NUMBER
2677	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,873	KIGO ET AL.	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/28/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2. 3/08/04, 7/21/04, 9-28-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai (USPN 6011355).

Regarding claim 1, 3, 8, 10 and 15-18, Nagai teaches a driving circuit that drives a display panel having an electrode, (Fig. a (1)) comprising: a switcher connected to a power supply; (Fig. 1(22a, 22b, Vcc) and interconnector connected to said switcher; and a frequency reducer connected in parallel with said switcher (Fig. 1 (LX, 22a, 22b), Fig. 36 (L) and col. 5, lines 38-65) that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said switcher and an inductance component of said interconnector, wherein a potential of said power supply is applied to the electrode of the display panel through said switcher and said interconnector. See col. 11, lines 65-66, col. 12, lines 1-36 and Fig. 15 (12).

Nagai does not specifically teach a frequency reducer. Nagai on the other hand teaches that when the inductance L is set to the value L3, the resonance frequency is the lowest and the Q-value is the highest. See col. 5, lines 38-65 and Fig. 36.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to manipulate inductance values with respect to Fig 1 to obtain the desired frequency.

Regarding claims 2, 6, 9 and 13, Nagai teaches a driving circuit that drives a display panel having an electrode, (Fig. a (1)) comprising: a switcher connected to a power supply; (Fig. 1(22a, 22b, Vcc) an interconnector connected to said switcher; and a frequency reducer connected in parallel with said switcher (Fig. 1 (LX, 22a, 22b), Fig. 36 (L) and col. 5, lines 38-65) that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said switcher and an inductance component of said interconnector to a level less than 30 MHz, wherein a potential of said power supply is applied to the electrode of the display panel through said switcher and said interconnector.

Nagai does not specifically teach a frequency reducer with respect to a reduction level of less than 30MHZ.

Nagai on the other hand teaches the reactive power recovery efficiency with respect to circuit in FIG. 33, and uses an equation to the reactive power P0 caused by the panel capacitance 12 having a capacitance value Cp as P0 = fxCp xVcc (squared) where f is the frequency of charging and discharging per unit time. See col. 4, lines 40-54

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize Nagai reactive power P0 equation for the purpose of setting the desired level of frequency.

Regarding claim 4, 5, 7, 11-12 and 14, Nagai teaches driving circuit that drives a display panel having an electrode, comprising: a switcher connected to a power supply; (Fig. 1 (22a, 22b, Vcc) a first interconnector connected to said switcher; a protector connected to said power supply; a second interconnector connected to said protector and said first interconnector; and a frequency reducing device connected in parallel with said protector (Fig. 1 (LX, 22a, 22b), Fig. 36 (L) and col. 5, lines 38-65) that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of said protector and an inductance component of said second interconnector, col. 11, lines 65-66, col. 12, lines 1-36 and Fig. 15 (12).wherein a potential of the electrode of the display panel is brought to a level that does not exceed a potential of said power supply through said protector and said second interconnector (Fig. 4 (107a) 102).

Nagai does not specifically teach frequency reducer. Nagai on the other hand teaches that when the inductance L is set to the value L3, the resonance frequency is the lowest and the Q-value is the highest. See col. 5, lines 38-65 and Fig. 36.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to manipulate inductance values with respect to Fig 1 to obtain the desired frequency.

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat. N0, 5,962,993 to Kashiwagi

U.S. Pat. No. 5,821,838 to Suzuki et al.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is (571) 272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard, can be reached on (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas Abdulselam

Examiner

Art Unit 2674

June 15, 2005

XIAO WU
PRIMARY EXAMINER